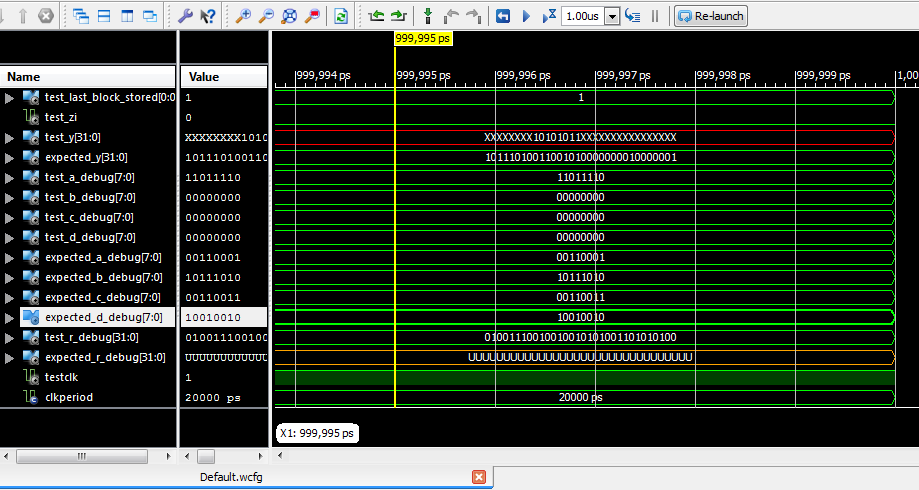
**Printout from Functional Simulation**

****

**Warnings after Synthesis**WARNING:Xst:647 - Input <i<5:4>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.  
WARNING:Xst:646 - Signal <Z<18:8>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.  
WARNING:Xst:646 - Signal <Y<17:8>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.  
WARNING:Xst:646 - Signal <X<15:8>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.  
WARNING:Xst:646 - Signal <D\_PLUS\_H3\_TEMP<8>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.  
WARNING:Xst:646 - Signal <C\_PLUS\_H2\_TEMP<8>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.  
WARNING:Xst:646 - Signal <B\_PLUS\_H1\_TEMP<8>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.  
WARNING:Xst:646 - Signal <A\_PLUS\_H0\_TEMP<8>> is assigned but never used. This unconnected signal will be trimmed during the optimization process. **Resource Utilization after Synthesis**Please note that I had to use a different device, as I was having trouble implementing at first under the smallest of the Spartan 3E families (too many I/O buffers). I tried to reduce this number, but I could not remove enough if I were to maintain the testbench.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Device Utilization Summary (estimated values)** | | | | **[-]** |
| **Logic Utilization** | **Used** | **Available** | **Utilization** | |
| Number of Slices | 99 | 8672 | 1% | |
| Number of Slice Flip Flops | 104 | 17344 | 0% | |
| Number of 4 input LUTs | 145 | 17344 | 0% | |
| Number of bonded IOBs | 140 | 190 | 73% | |
| Number of MULT18X18SIOs | 2 | 28 | 7% | |
| Number of GCLKs | 1 | 24 | 4% | |

**Maximum Clock Frequency After Synthesis**The minimum period is 9.825ns, thus the maximum frequency is 101.783 MHz after synthesis.

**Printout from Post-Synthesis Simulation(in folder)**

**Resource Utilization after Implementation**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Device Utilization Summary** | | | | | **[-]** |
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Flip Flops | 104 | 17,344 | 1% |  | |
| Number of 4 input LUTs | 144 | 17,344 | 1% |  | |
| Number of occupied Slices | 95 | 8,672 | 1% |  | |
| Number of Slices containing only related logic | 95 | 95 | 100% |  | |
| Number of Slices containing unrelated logic | 0 | 95 | 0% |  | |
| Total Number of 4 input LUTs | 152 | 17,344 | 1% |  | |
| Number used as logic | 144 |  |  |  | |
| Number used as a route-thru | 8 |  |  |  | |
| Number of bonded IOBs | 140 | 190 | 73% |  | |
| IOB Flip Flops | 33 |  |  |  | |
| Number of BUFGMUXs | 1 | 24 | 4% |  | |
| Number of MULT18X18SIOs | 2 | 28 | 7% |  | |
| Average Fanout of Non-Clock Nets | 3.00 |  |  |  | |

**Maximum Clock Frequency after Implementation**  
The minimum clock period is 9.327ns, and so the maximum clock frequency is 107.22MHz.  **Critical Path (text format)**

[Maximum Data Path: Count\_I/Count\_0\_1 to REG\_A/Q\_7](CPPath%5eMaximum%20Data%20Path:%20Count_I/Count_0_1%20to%20REG_A/Q_7%5eBel,Count_I/Count_0_1,0.511,Net,Count_I/Count_0_1,0.592,Bel,RND/Mmux_ri_33,1.000,Bel,RND/Mmux_ri_2_f5_2,NA,Net,RND/ri%3c3%3e,0.566,Bel,RND/Madd_X_Madd_xor%3c7%3e121_SW0,0.612,Net,RND/Madd_X_Madd_xor%3c7%3e121_SW0/O,0.020,Bel,RND/Madd_X_Madd_xor%3c7%3e12,0.612,Net,RND/X%3c7%3e,0.516,Bel,RND/Mmult_Y,3.861,Net,RND/Y%3c7%3e,0.309,Bel,MUX_4_OUT%3c7%3e1,0.728,Bel,REG_A/Q_7,NA)

Location Delay type Delay(ns) Physical Resource

Logical Resource(s)

------------------------------------------------- -------------------

SLICE\_X3Y52.YQ [Tcko](delayNameHelp%5eTcko%5espartan3e) 0.511 Count\_I/Count\_0\_1

[Count\_I/Count\_0\_1](CPBel%5eCount_I/Count_0_1,0.511%5eCount_I/Count_0_1,0.511)

SLICE\_X0Y50.F3 net (fanout=12) 0.592 [Count\_I/Count\_0\_1](CPNetPath%5eCount_I/Count_0_1%5eBel,Count_I/Count_0_1,0.511,Net,Count_I/Count_0_1,0.592,Bel,RND/Mmux_ri_33,1.000)

SLICE\_X0Y50.X [Tif5x](delayNameHelp%5eTif5x%5espartan3e) 1.000 RND/ri<3>

[RND/Mmux\_ri\_33](CPBel%5eRND/Mmux_ri_33,1.000%5eRND/Mmux_ri_33,1.000)

[RND/Mmux\_ri\_2\_f5\_2](CPBel%5eRND/Mmux_ri_2_f5_2,NA%5eRND/Mmux_ri_2_f5_2,NA)

SLICE\_X3Y57.G2 net (fanout=2) 0.566 [RND/ri<3>](CPNetPath%5eRND/ri%3c3%3e%5eBel,RND/Mmux_ri_2_f5_2,NA,Net,RND/ri%3c3%3e,0.566,Bel,RND/Madd_X_Madd_xor%3c7%3e121_SW0,0.612)

SLICE\_X3Y57.Y [Tilo](delayNameHelp%5eTilo%5espartan3e) 0.612 RND/X<7>

[RND/Madd\_X\_Madd\_xor<7>121\_SW0](CPBel%5eRND/Madd_X_Madd_xor%3c7%3e121_SW0,0.612%5eRND/Madd_X_Madd_xor%3c7%3e121_SW0,0.612)

SLICE\_X3Y57.F4 net (fanout=1) 0.020 [RND/Madd\_X\_Madd\_xor<7>121\_SW0/O](CPNetPath%5eRND/Madd_X_Madd_xor%3c7%3e121_SW0/O%5eBel,RND/Madd_X_Madd_xor%3c7%3e121_SW0,0.612,Net,RND/Madd_X_Madd_xor%3c7%3e121_SW0/O,0.020,Bel,RND/Madd_X_Madd_xor%3c7%3e12,0.612)

SLICE\_X3Y57.X [Tilo](delayNameHelp%5eTilo%5espartan3e) 0.612 RND/X<7>

[RND/Madd\_X\_Madd\_xor<7>12](CPBel%5eRND/Madd_X_Madd_xor%3c7%3e12,0.612%5eRND/Madd_X_Madd_xor%3c7%3e12,0.612)

MULT18X18\_X0Y7.B7 net (fanout=1) 0.516 [RND/X<7>](CPNetPath%5eRND/X%3c7%3e%5eBel,RND/Madd_X_Madd_xor%3c7%3e12,0.612,Net,RND/X%3c7%3e,0.516,Bel,RND/Mmult_Y,3.861)

MULT18X18\_X0Y7.P7 [Tmult](delayNameHelp%5eTmult%5espartan3e) 3.861 RND/Mmult\_Y

[RND/Mmult\_Y](CPBel%5eRND/Mmult_Y,3.861%5eRND/Mmult_Y,3.861)

SLICE\_X3Y60.F4 net (fanout=1) 0.309 [RND/Y<7>](CPNetPath%5eRND/Y%3c7%3e%5eBel,RND/Mmult_Y,3.861,Net,RND/Y%3c7%3e,0.309,Bel,MUX_4_OUT%3c7%3e1,0.728)

SLICE\_X3Y60.CLK [Tfck](delayNameHelp%5eTfck%5espartan3e) 0.728 REG\_A/Q<7>

[MUX\_4\_OUT<7>1](CPBel%5eMUX_4_OUT%3c7%3e1,0.728%5eMUX_4_OUT%3c7%3e1,0.728)

[REG\_A/Q\_7](CPBel%5eREG_A/Q_7,NA%5eREG_A/Q_7,NA)